50. The ATM switch according to claim 42, wherein the data buffers are physically associated with output ports.

51. The ATM switch according to claim 42, wherein the rate limitation is enforced at inputs.

52. The ATM switch according to claim 42, wherein the rate limitation is enforced at outputs.

53. (Amended) The ATM switch according to claim 42, wherein an input port and the determination of whether the additional data units which designate relatively low priorities and a particular input port are in violation of the rate limitation is based on a "leaky bucket" algorithm.

54. The ATM switch according to claim 53, wherein the particular input port is associated with a selected store whose backlog caused the selective filtering condition to be imposed.

REMARKS

Claims 1-5, 7-16 and 18-54 are pending in the present application, of which claims 1, 10, 23, 33 and 42 are independent, and claims 23-32 have been allowed. Applicants appreciate the allowance of claims 23-32 and the approval of the proposed drawing correction filed on April 15, 2002. Claims 1-4, 10, 13-15, 21, 33-36, 42, 45-47 and 53 have been amended herein. Applicants respectfully submit that the amendment places the application in form for allowance without requiring any further search. Hence, applicants respectfully request that the amendment be entered and further request reconsideration and allowance of claims 1-5, 7-16, 18-22 and 33-54 in addition to the allowed claims 23-32.

The Examiner has rejected claims 1, 5, 7-10, 16, 18-20 and 22 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,046,981 to Ramamurthy et al. ("Ramamurthy"). In addition, the Examiner has rejected claims 2-4, 11-15 and 21 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ramamurthy in view of U.S. Patent No. 5,497,375 to Hluchyj et al. ("Hluchyj"). Further, the Examiner has rejected claims 33, 37-42,

48-52 and 54 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ramamurthy in view of U.S. Patent No. 6,122,251 to Shinohara ("Shinohara"). The Examiner has also rejected claims 34-36, 43-47 and 53 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ramamurthy in view of Shinohara and further in view of Hluchyj.

According to the Examiner, Ramamurthy discloses a switch comprising a plurality of input ports, a plurality of output ports and switch fabric, wherein the output data stores on the output side are arranged to buffer data units for delivery to output ports, and if the backlog reaches a particular level, to enforce rate limitation, wherein the additional data units in violation of the rate limitation are filtered.

In this determination, the Examiner appears to equate the "CAC" [bandwidth allocator] of FIG. 1 in Ramamurthy with the "output control" of the present application. Applicants respectfully traverse this finding by the Examiner since the output control performs at least one function that CAC does not. Nowhere does Ramamurthy discloses that the CAC is used to segregate the data units for storage in the output data stores based on their designated priorities at the output end. Instead, it appears that the overall capacity of the input buffer in Ramamurthy is partitioned between different classes at the input end (Col. 4, lines 23-30).

Applicants have amended some of the claims to clarify this patentably distinguishable feature of the output control. For example, each of claims 1, 10, 33 and 42 now recites, in relevant portion, that "the output controls are arranged to segregate the data units for storage in the output data stores based on their designated priorities." This clarification is supported, for example, by the specification of the present application on page 8, lines 5-8. Since Ramamurthy does not disclose that the output controls are arranged to segregate the data units for storage in the output data stores based on their designated priorities, applicants respectfully request that the rejection of claims 1, 10, 33 and 42 be withdrawn and that they be allowed.

Since claims 2-5, 7-9, 11-16, 18-22 and 34-41 and 43-54 depend, directly or indirectly, from claims 1, 10, 33 and 42, respectively, they incorporate all the terms and limitations of the claims from which they depend, in addition to other limitations, which together patentably

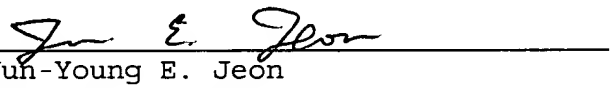
distinguish them over the cited references. Therefore, applicants respectfully request that the rejection to claims 2-5, 7-9, 11-16, 18-22 and 34-41 and 43-54 be withdrawn and that they be allowed.

In view of the foregoing amendments and remarks, applicants respectfully request the allowance of claims 1-5, 7-16, 18-22 and 33-54 in addition to the already allowed claims 23-32. If there are any remaining issues that can be discussed over the phone, the Examiner is invited to call applicants' attorney at the number listed below.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By 

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VERSION TO SHOW CHANGES MADE

In the Claims:

1. (Thrice Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections, each of the data units designating a priority;

a plurality of output ports, each output port operatively associated with a plurality of output data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the output data stores on an output side of the switch fabric are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to segregate the data units for storage in the output data stores based on their designated priorities and to monitor the backlog of buffered data units in one or more of said plurality of output data stores for delivery to their associated output ports and, if the backlog reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

2. (Amended) The ATM switch according to claim 1, wherein [~~each of the data units designates a priority and~~] the additional data units which designate relatively high priorities are not in violation of the rate limitation.

3. (Amended) The ATM switch according to claim 1, wherein [~~each of the data units designates a priority and~~] the additional data units which designate relatively low priorities are in violation of the rate limitation.

4. (Amended) The ATM switch according to claim 1, wherein [~~each of the data units designates a priority and~~] the determination of whether the additional data units which designate relatively low priorities are in violation of the rate limitation is based on a "leaky bucket" algorithm.

10. (Thrice Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections, each of the data units designating a priority;

a plurality of output ports, each output port operatively associated with a plurality of output data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the output data stores on an output side of the switch fabric are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to segregate the data units for storage in the output data stores based on their designated priorities and to monitor the backlog of buffered data units in one or more of said plurality of output data stores for delivery to their associated output ports and, if the backlog buffered in one or more selected stores reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

13. (Amended) The ATM switch according to claim 10, wherein [~~each of the data units designates a priority and~~] the additional data units which designate relatively high priorities are not in violation of the rate limitation.

14. (Amended) The ATM switch according to claim 10, wherein [~~each of the additional data units designates a priority and~~] the additional data units which designate relatively low priorities are in violation of the rate limitation.

15. (Amended) The ATM switch according to claim 10, wherein [~~each of the data units designates a priority and~~] the determination of whether the additional data units which designate relatively low priorities are in violation of the rate limitation is based on a "leaky bucket" algorithm.

21. (Amended) The ATM switch according to claim 10, wherein [~~each of the data units designates a priority and~~] an input port and the

determination of whether the additional data units which designate relatively low priorities and a particular input port are in violation of the rate limitation is based on a "leaky bucket" algorithm.

33.(Twice Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections, each of the data units designating a priority;

a plurality of output ports, each output port operatively associated with a plurality of data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to segregate the data units for storage in the output data stores based on their designated priorities and to monitor the backlog of buffered data units buffered in two or more of said plurality of data stores for delivery to their associated output ports and, if the backlog reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

34. (Amended) The ATM switch according to claim 33, wherein [~~each of the data units designates a priority and~~] the additional data units which designate relatively high priorities are not in violation of the rate limitation.

35. (Amended) The ATM switch according to claim 33, wherein [~~each of the data units designates a priority and~~] the additional data units which designate relatively low priorities are in violation of the rate limitation.

36. (Amended) The ATM switch according to claim 33, wherein [~~each of the data units designates a priority and~~] the determination of whether the additional data units which designate relatively low priorities are in violation of the rate limitation is based on a "leaky bucket" algorithm.

42.(Twice Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections, each of the data units designating a priority;

a plurality of output ports, each output port operatively associated with a plurality of data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to segregate the data units for storage in the output data stores based on their designated priorities and to monitor the backlog of buffered data units buffered in two or more of said plurality of data stores for delivery to their associated output ports and, if the backlog buffered in one or more selected stores reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

45. (Amended) The ATM switch according to claim 42, wherein [~~each of the data units designates a priority and~~] the additional data units which designate relatively high priorities are not in violation of the rate limitation.

46. (Amended) The ATM switch according to claim 42, wherein [~~each of the additional data units designates a priority and~~] the additional data units which designate relatively low priorities are in violation of the rate limitation.

47. (Amended) The ATM switch according to claim 42, wherein [~~each of the data units designates a priority and~~] the determination of whether the additional data units which designate relatively low priorities are in violation of the rate limitation is based on a "leaky bucket" algorithm.

53. (Amended) The ATM switch according to claim 42, wherein [~~each of the data units designates a priority and~~] an input port and the determination of whether the additional data units which designate relatively low priorities and a particular input port are in violation of the rate limitation is based on a "leaky bucket" algorithm.